What is claimed is:

1. A circuit that is capable of providing stable timing clock, includes:

a step-down clamping circuit which has an input side to input first voltage, and an output side to output second voltage. The first voltage passing step down and clamp to output second voltage.

an oscillating circuit, which is coupled to the clamping circuit and is an oscillating circuit that takes the second voltage as a operating voltage to further generate a first timing clock signal, which has a lower voltage potential; and

a voltage potential-conversing circuit, which is coupled to the oscillating circuit to convert the first timing clock signal into a second timing clock signal, which has a higher voltage potential.

2. The circuit according to claim 1, wherein the first voltage is characterized in that there are large variations for both rippling wave and voltage potential.

3. The circuit according to claim 1, wherein the second voltage is an ideal DC voltage.

4. The circuit according to claim 1, wherein the second voltage is smaller than the first voltage.

5. The circuit according to claim 1, wherein the step-down clamping circuit further includes: a resistance, a capacitance, and a clamping circuit.

6. The circuit according to claim 5, wherein the clamping circuit includes a P-type metal oxide semiconductor PMOS and an N-type metal oxide semiconductor NMOS.

7. A circuit capable of providing stable timing clock, includes:

a rectifying circuit, which may convert an AC voltage into a DC voltage that is a first voltage;

a step-down clamping circuit, which is coupled to the rectifying circuit to receive the first voltage, and which is able to output a second voltage;

an oscillating circuit, which is coupled to the clamping circuit and is an oscillating circuit that takes the second voltage as a operating voltage to further generate a first timing clock signal, which has a lower voltage potential; and

a voltage potential-conversing circuit, which is coupled to the oscillating circuit to convert the first timing clock signal into a second timing clock signal, which has a higher voltage potential.

8. The circuit according to claim 7, wherein the first voltage is characterized in that there are large variations for both rippling wave and voltage potential.

9. The circuit according to claim 7, wherein the rectifying circuit is comprised of a rectifier, a filter, and a voltage limiter.

10. The circuit according to claim 7, wherein the second voltage is an ideal DC voltage.

11. The circuit according to claim 7, wherein the second voltage is smaller than the first voltage.

12. The circuit according to claim 7, wherein the step-down clamping circuit further includes: a resistance, a capacitance, and a clamping circuit.

13. The circuit according to claim 12, wherein the clamping circuit includes a P-type metal oxide semiconductor (PMOS) and an N-type metal oxide semiconductor (NMOS).